TecNews: Sandy Bridge

Werner Fischer, Technology Specialist Thomas-Krenn.AG

Thomas Krenn Herbstworkshop & Roadshow 2011

23.09. in Freyung
06.10. in Wien (A)
10.10. in Frankfurt
11.10. in Düsseldorf
12.10. in Hamburg
13.10. in Berlin
19.10. in München
20.10. in Zürich (CH)
25.10. in Prag (CZ)

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Speed is (y)our success

Agenda

1) **Tick – Tock Modell**
2) **Neuheiten**
3) **Single Socket Systeme**
4) **Dual Socket Systeme**
5) **Ausblick Ivy Bridge**

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1) **Tick – Tock Modell**

2) Neuheiten

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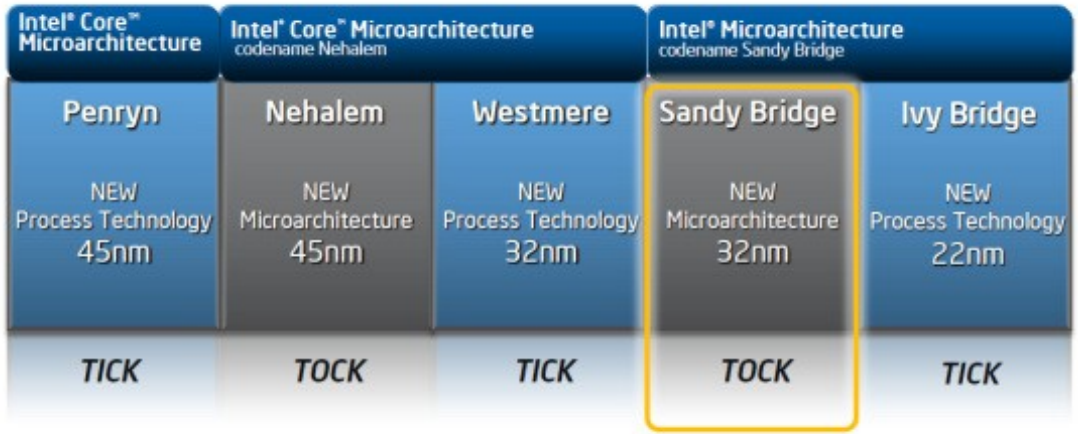
1) Tick – Tock Modell



	Merom (65nm)	Penryn	Nehalem	Westmere	Sandy Bridge	Ivy Bridge
single CPU (EN)	Xeon 32xx	Xeon 33xx	Xeon 34xx	Xeon 36xx	Xeon E3-12xx	?
dual CPU (EN)					Xeon E5-24xx	?
dual CPU (EP)	Xeon 51xx 53xx	Xeon 52xx 54xx	Xeon 55xx	Xeon 56xx	Xeon E5-26xx	?

Systeme bereits verfügbar

Weitere Informationen:
http://www.thomas-krenn.com/de/wiki/Intel_CPUs_im_Überblick

Agenda

1) Tick – Tock Modell

2) **Neuheiten**

- **Full Integration**
- **Next Generation Intel Turbo Boost**
- **Doppelte Load Bandwidth im Memory Cluster**
- **Advanced Vector Extenstions (AVX)**

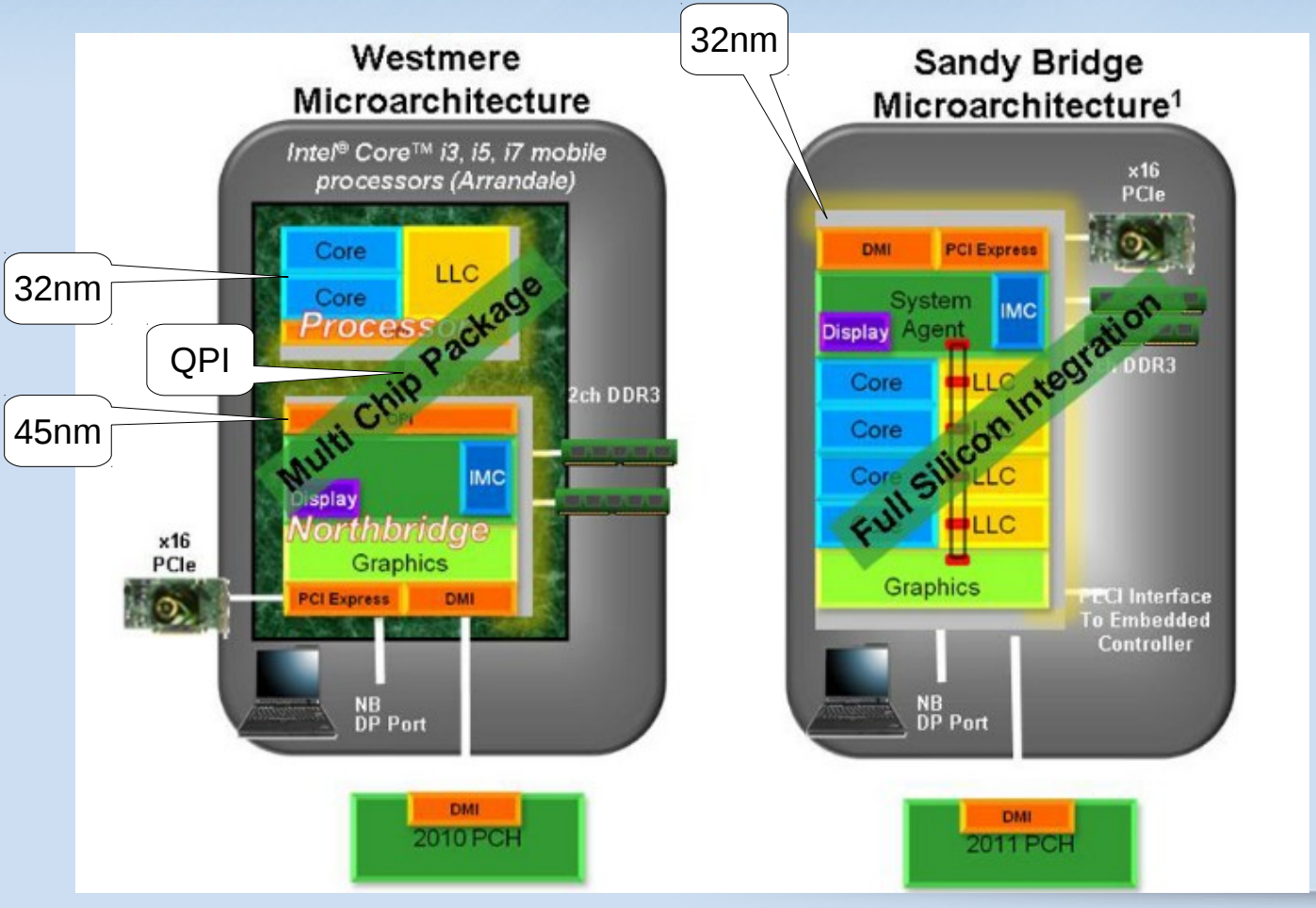
3) Single Socket Systeme

4) Dual Socket Systeme (Romley Platform)

5) Ausblick Ivy Bridge

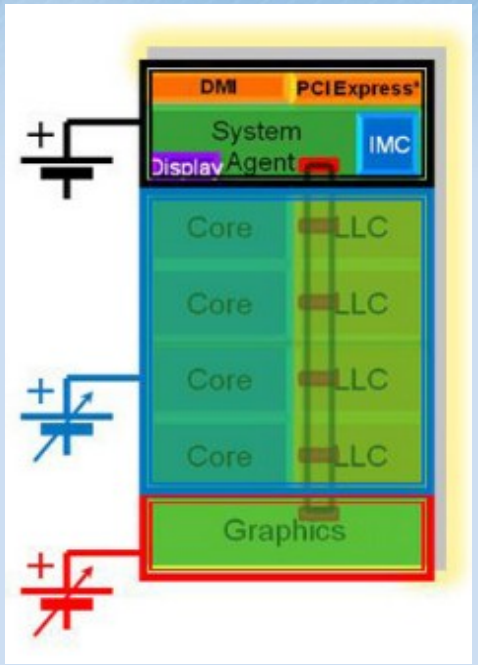
2) Neuheiten

- **Full Integration: one chip design vs. one package design**



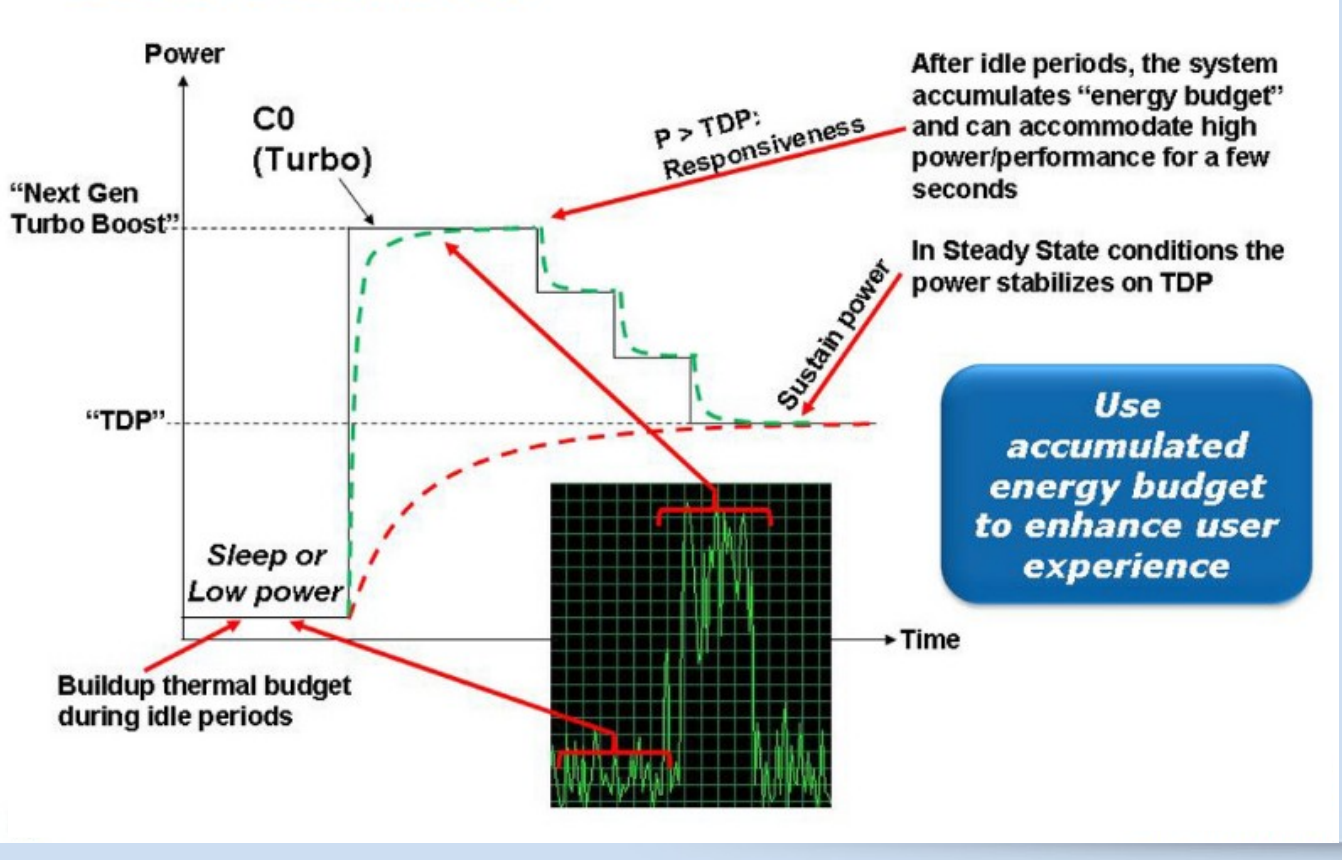
2) Neuheiten

- **Full Integration:**
  - High Bandwidth Last Level Cache (LLC), für Cores und Grafik
  - High Bandwith / Low Latency Ring Interc.
  - System Agent
    - Memory Controller (Integration spart Energie, da keine Bus-Anbindung mehr nötig)
    - PCIe
    - Display (unabhängig vom Grafik Core)
    - Power Control Unit
  - drei separate Voltage Domains, zwei davon variabel
  - höhere Performance bei weniger Energie



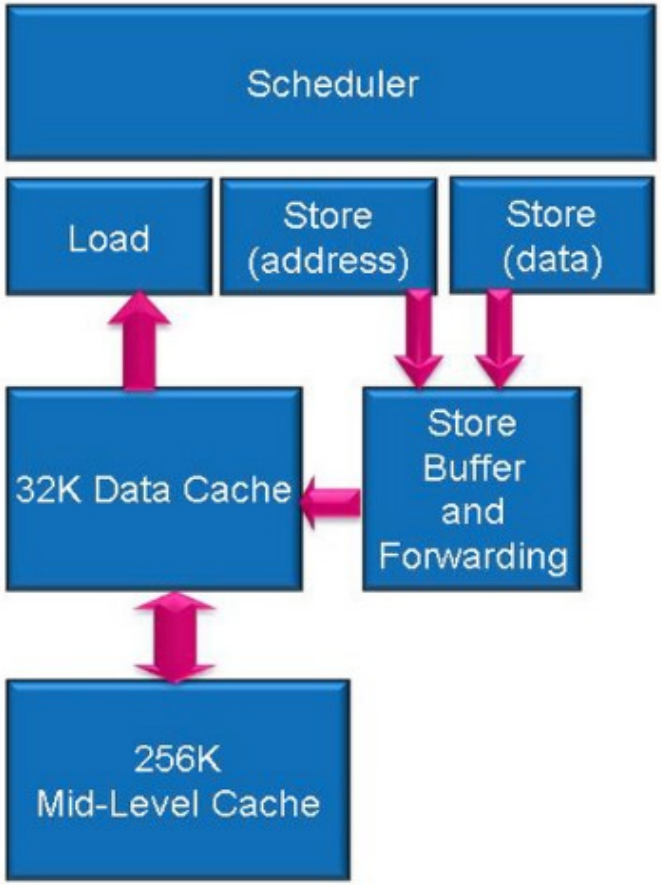
2) Neuheiten

- **Next Generation Intel Turbo Boost**
  - Strom (Ampere) geht kurz über TDZ, CPU ist hier aber noch kühl



2) Neuheiten

- **Doppelte Load Bandwidth im Memory Cluster, zuvor:**

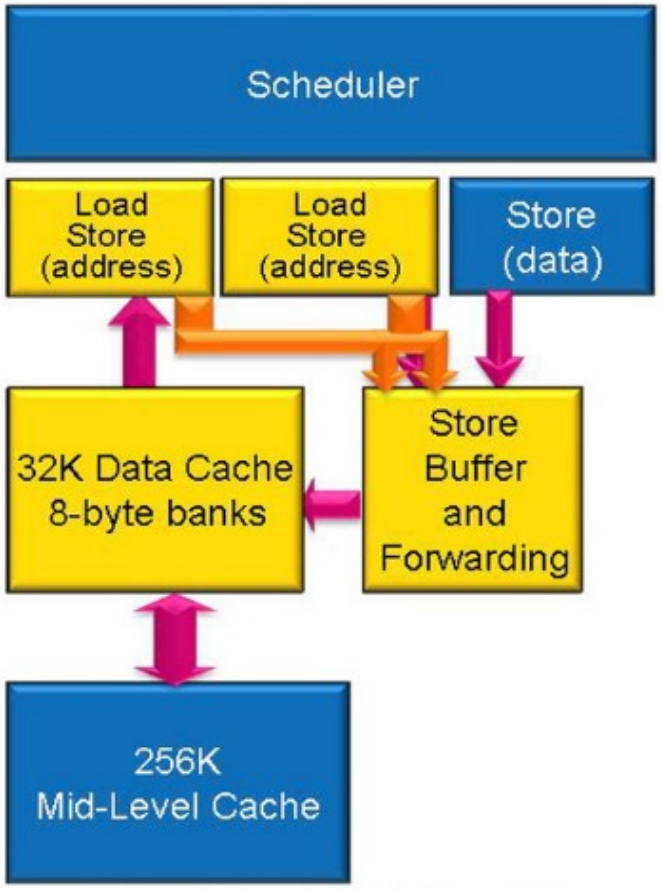


Start with the memory execution unit used in the Nehalem Microarchitecture

- 32K Data Cache
- 256K mid-level cache
- Excellent prefetchers and memory hazard handling
- Excellent misalignment support
- Support many store-forwarding scenarios

2) Neuheiten

- **Doppelte Load Bandwidth im Memory Cluster, nun:**



2 loads per cycle increases performance for many applications

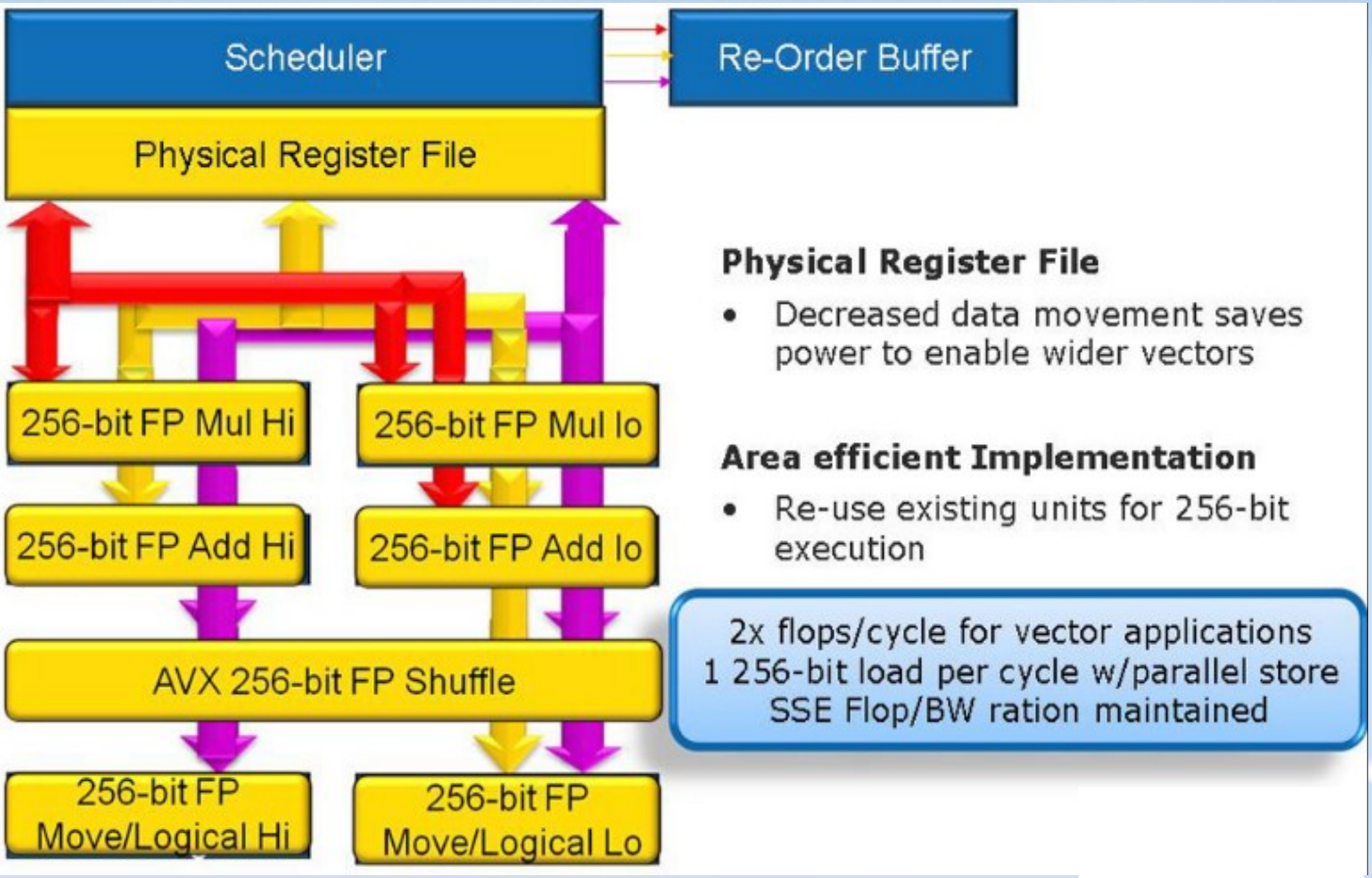
Make the memory ports symmetric

- Two 128-bit loads per cycle
- *Second load port is fully featured for misalignment and store forwarding*
- Increased store address BW

48 bytes per cycle internal memory bandwidth

2) Neuheiten

- **Advanced Vector Extensions (AVX)**



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3) Single Socket Systeme

- **Eigenschaften Server vs. Desktop:**
  - ECC Support
  - 20 PCIe 2.0 Lanes (statt 16)
  - vier Memory Controller (statt drei)
  - keine integrierte Grafik

- **Vergleich zu Nehalem/Westmere**
  - zwei SATA 6Gbit/s Ports am Platform Controller Hub (bei C204 und C206 Chipset)
  - System Agent in der CPU, kein QPI mehr nötig

Weitere Informationen:
http://www.thomas-krenn.com/de/wiki/Sandy_Bridge#Neuheiten_bei_Single-CPU_Systemen

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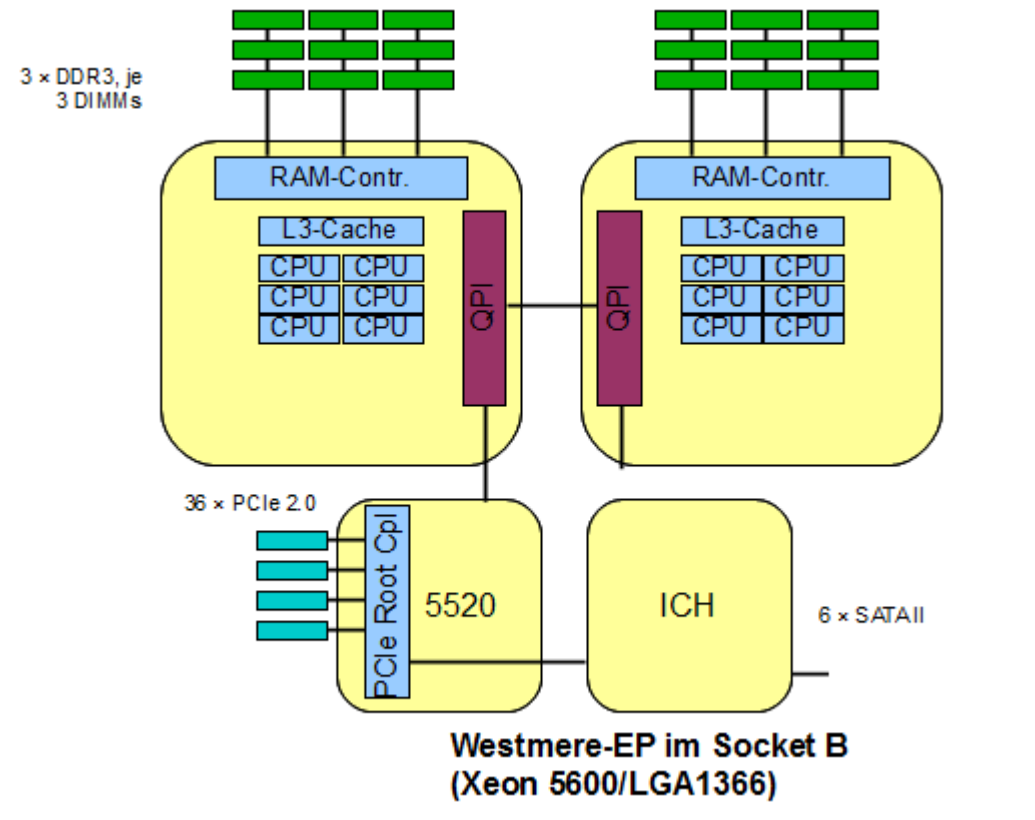
4) Dual Socket Systeme (Romley Platform)

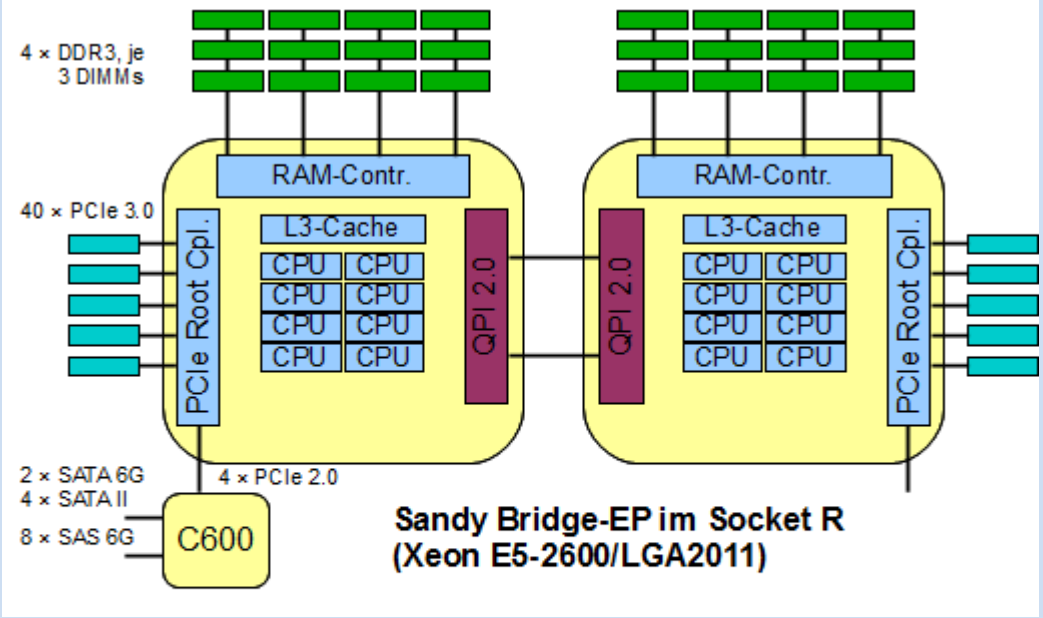
- **Westmere-EP (Nehalem Microarchitecture)**
  - PCIe Root Complex im Chipsatz (angebunden per QPI):



Quelle: http://heise.de/-1253138

4) Dual Socket Systeme (Romley Platform)

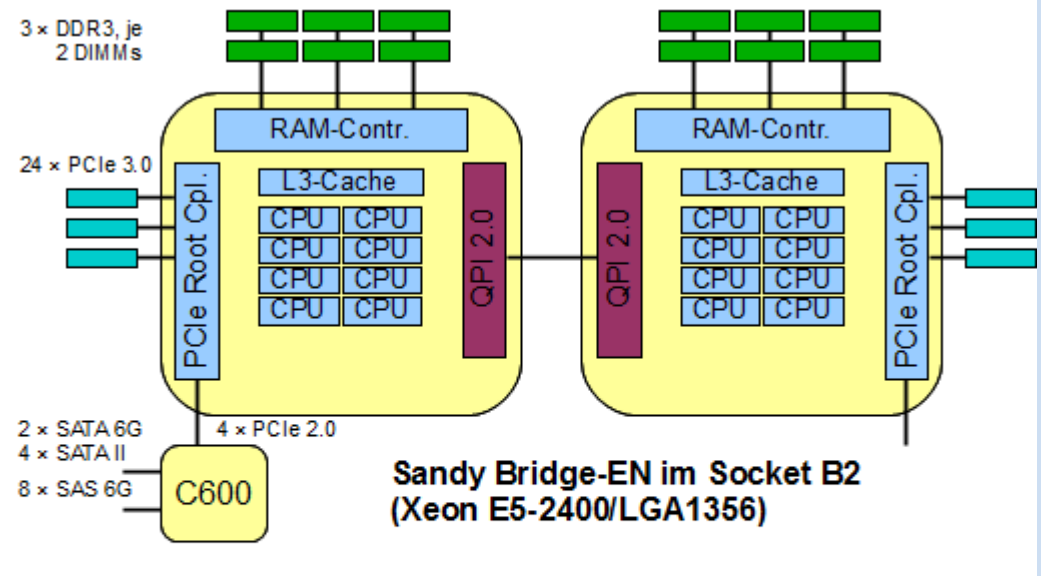
- **Sandy Bridge-EP (Romley Platform, ETA TBA)**
  - PCIe Root Complex in der CPU (spart Energie)
  - zwei QPI 1.1 Links zwischen CPUs
  - 2 x 40 x PCIe 3.0 und 2 x 4 x DDR3 Channels á 3 DIMMs



Quelle: http://heise.de/-1253138

4) Dual Socket Systeme (Romley Platform)

- **Sandy Bridge-EN (Romley Platform, ETA TBA)**
  - PCIe Root Complex in der CPU (spart Energie)
  - ein QPI 1.1 Link zwischen CPUs
  - 24 x PCIe 3.0 und 3 x DDR3 Channels á 2 DIMMs (pro CPU)



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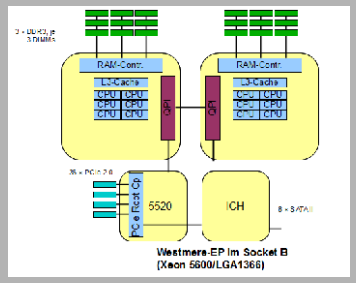
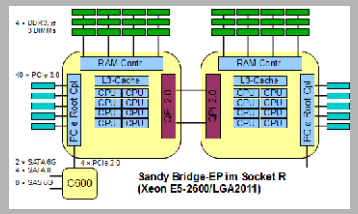
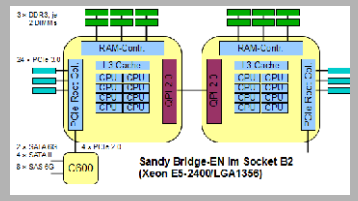
4) Dual Socket Systeme (Romley Platform)

	Westmere-EP	Sandy Bridge-EP	Sandy Bridge-EN
			
		(Romley)	(Romley)
PCIe Root Cplx	Chipsatz	CPU	CPU
PCIe Lanes	36x PCIe 2.0	80x PCIe 3.0	48x PCIe 3.0
Memory Channels	3x DDR3, á 3 DIMMS / CPU	4x DDR3, á 3 DIMMS / CPU	3x DDR3, á 2 DIMMS / CPU
CPU Interlink	QPI 1.0	2x QPI 1.1	QPI 1.1
Cores	max. 6	max. 8	max. 8

Weitere Informationen:
http://heise.de/-1253138
http://www.realworldtech.com/page.cfm?ArticleID=RWT072811020122

4) Dual Socket Systeme (Romley Platform)

- **PCIe (Peripheral Component Interconnect Express)**

	PCIe 1.0/1.1	PCIe 2.0/2.1	PCIe 3.0
GT (pro Lane)	2,5	5,0	8,0
Kodierung	8b/10b	8b/10b	128b/130b
Datenrate x1	250 MB/s	500 MB/s	1 GB/s
Datenrate x8, Beispiele	2 GB/s Adaptec Series-5 LSI 3Gb/s SAS	4 GB/s Adaptec Series-6 LSI 6Gb/s SAS	8 GB/s
Datenrate x16	4 GB/s	8 GB/s	16 GB/s

(Datenraten sind full duplex)

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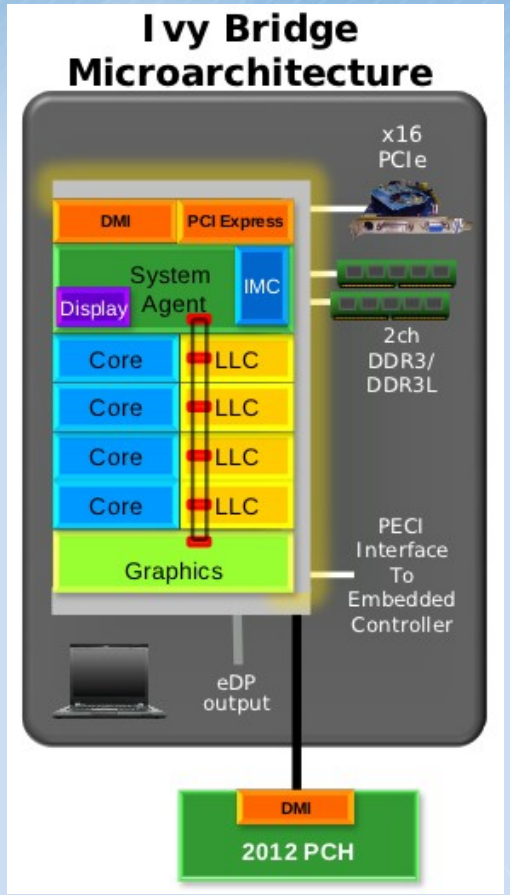
5) Ausblick Ivy Bridge

- **22nm statt 32nm**
  - Mehr Performance, weniger Energie
- **verbesserte Grafik/Media („Tick+“)**
  - drei Displays
  - DirectX 11
- **Dig. Random Number Gen.**
- **Power Aware Interrupt Routing**
- **Konfigurierbarer TDP**
  - dynamische Übergänge
  - Bsp. Laptop Netzteil/Akku-Betrieb



Sandy Bridge ist ein weiterer Schritt zu höherer Performance und weniger Energiebedarf

Single CPU Systeme bereits verfügbar

Ivy Bridge wird Trend fortsetzen